MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Fall 2002

Quiz 2

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Enter all your work and your answers directly in the spaces provided on the printed pages. Make sure that your name is on all sheets. Use the backs of the printed pages as scratch paper, but we will only grade the work that you neatly transfer to the spaces on the printed pages. Answers must be derived or explained, not just simply written down. The quiz is closed book, but **calculators are allowed.**

This quiz contains 8 pages including the cover sheet. Make sure that your quiz contains all 8 pages and that you hand in all 8 pages.

Problem	Points	Grade	Grader
1	50	50	V.S.
2	50	50	
Total	100	100	V.S.

Problem 1: (*50 points*) Figure 1(a) shows a simple one-stage MOSFET amplifier. The input-output relationship is graphed in Figure 1(b), where the solid curve indicates operation in the saturated region and the dashed curves indicate operation in the cutoff and triode regions.

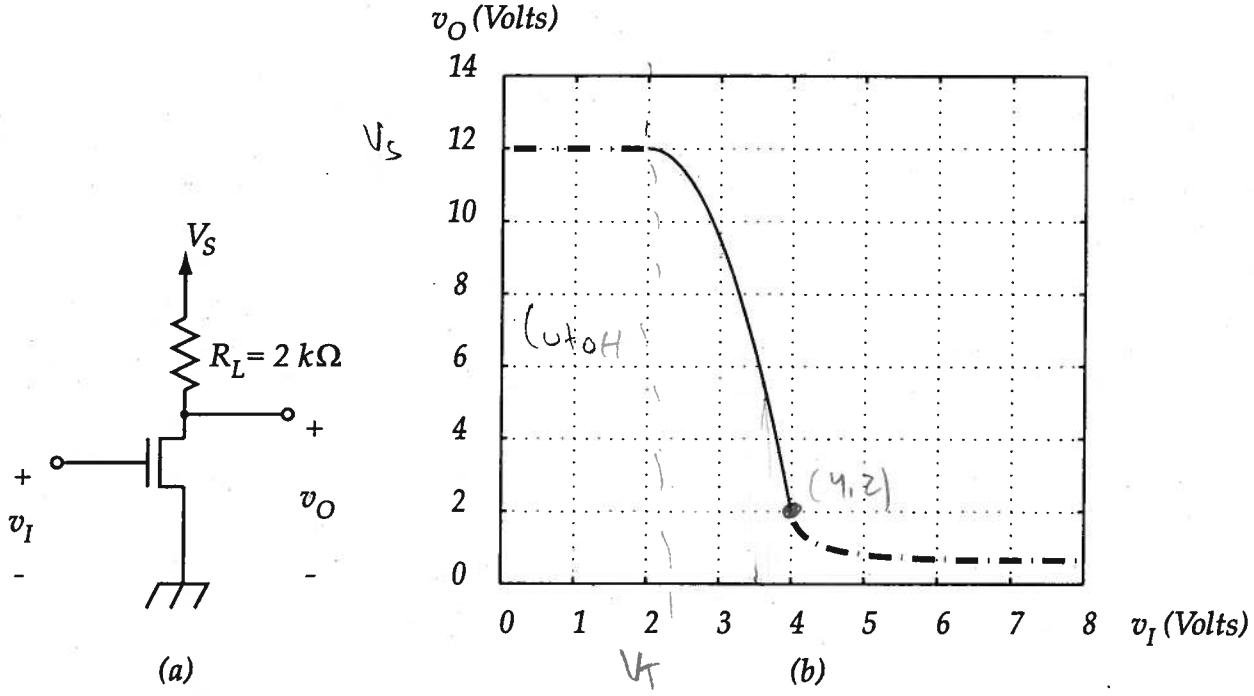

Figure 1: Circuit and characteristic for Problem 1

(A) Determine the MOSFET threshold voltage V_T and the power supply voltage V_S.

$V_T =$ 2 V

$V_S =$ 12 V

(B) Determine the MOSFET parameter K.

$K =$ 5/2 mA/V²

$v_{out} = V_S - \frac{R_L}{2}(V_{in} - V_T)^2$

$2V = 12V - \frac{2k\Omega}{2}(4V - 2V)^2$

$10V = K(2V)^2$

$K = 10/4\ mA/V^2 = 5/2\ mA/V^2$

(C) Determine the minimum and maximum small-signal gain $|\frac{v_o}{v_i}|$ in the saturated region. A graphical solution is acceptable.

$\left|\frac{v_o}{v_i}\right| = \frac{d}{dv_I} v_O \Big|_{V_I} = -2k(V_I - V_T)$

$= -\frac{2k\Omega \cdot 5/2\ mA/V^2}{2}(V_I - V_T)$

$= -5/4 \cdot (V_I - 2V)$

min $|\frac{v_o}{v_i}| =$ 0 at $V_I = 2V$

max $|\frac{v_o}{v_i}| =$ 1.0 at $V_I = 4V$

min at $V_I = 2V$

max at $V_I = 4V$

The circuit shown in Figure 2 is used to bias the amplifier and inject an input signal to be amplified. The values of R_1 and R_2 are to be determined.

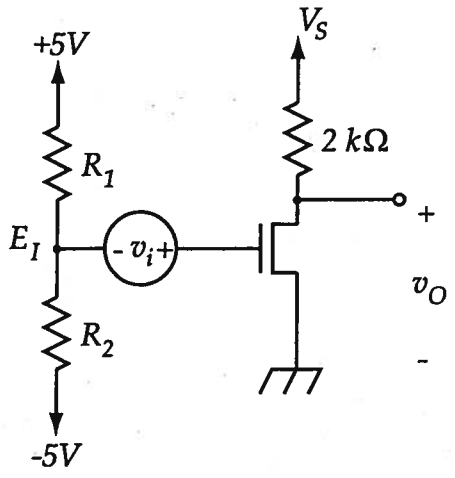

Figure 2: Circuit for Problem 1(D), where $v_O = V_O + v_o$

(D) Determine the bias voltage E_I (with respect to ground) such that equal positive and negative excursions of v_o can be as large as possible without leaving the saturation region.

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Choose V_O midway between its max and min values in saturation

$V_O = \frac{12V+2V}{2} = 7V$

$V_O = 12V - \frac{R_L}{2}(V_I - V_t)^2$

$7V = 12V - \frac{2k\Omega \cdot .5mA}{2 \cdot V^2}(E_I - 2V)^2$

$\Rightarrow 5V = .5/2 \frac{V}{V^2}(E_I - 2V)^2$

$2V^2 = (E_I - 2V)^2$

$\sqrt{2}V = E_I - 2V \Rightarrow E_I = (2+\sqrt{2})V$

$E_I = \underline{(2+\sqrt{2})V = 3.414V}$

(E) The resistors in Figure 2 satisfy the constraint $R_1 + R_2 = 10k\Omega$. Determine values for R_1 and R_2 so that the bias voltage E_I will be that found in part (D).

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$(5V - -5V)\frac{R_2}{R_1+R_2} = E_I - -5V \Rightarrow 10V\left(\frac{R_2}{R_1+R_2}\right) = E_I + 5V$

$10V\left(\frac{R_2}{R_1+R_2}\right) = E_I + 5V$

$R_1 + R_2 = 10k\Omega$, so

$10V\left(\frac{R_2}{10k\Omega}\right) = E_I + 5V$

$R_2 = \frac{10k\Omega}{10V}(E_I + 5V)$

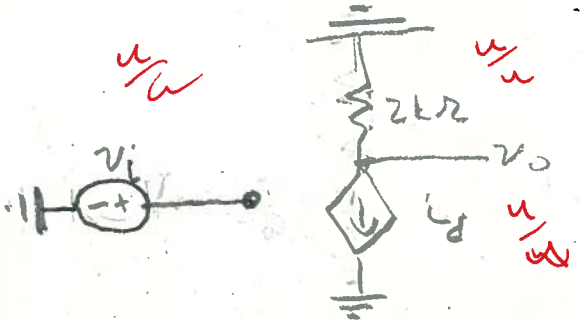
$= \frac{10k\Omega}{10V}(8.414V) = 8.414k\Omega$

$R_1 = 10k\Omega - R_2 = 1.586k\Omega$

$R_1 = \underline{1.586\ k\Omega}$

$R_2 = \underline{8.414\ k\Omega}$

15 (F) Draw the small-signal circuit valid for the operating point defined in part (D). Label the numerical values of all circuit parameters and determine the small-signal gain at this operating point from your circuit.



$v_o = 0 - 2k\Omega \cdot i_d$

$= -2k\Omega \cdot K(V_I - V_T) v_i$

$= -2k\Omega \cdot \frac{5}{2}\frac{mA}{V^2}(3.414V - 2V) v_i$

$= -5\sqrt{2} \cdot v_i = -7.07 v_i$

$i_d = K(V_I - V_T) v_i$

$V_I = E_I$

$K = 5/2\ mA/V^2$

$V_T = 2V$

$$\frac{v_o}{v_i} = -5\sqrt{2} = -7.07$$

In the small-signal model, the voltage sources used to bias the MOSFET are disabled so no current flows through the resistors R_1 and R_2. The bias portion of the circuit can thus be ignored. It is not drawn above.

great job!

Problem 2: (*50 points*) The circuit of Figure 3 is a model for a proposed logic inverter which is to join a logic family whose members must satisfy the following digital discipline:

$$V_{IH} = 3.3V \quad V_{OH} = 4.0V$$
$$V_{IL} = 1.55V \quad V_{OL} = 1.0V$$

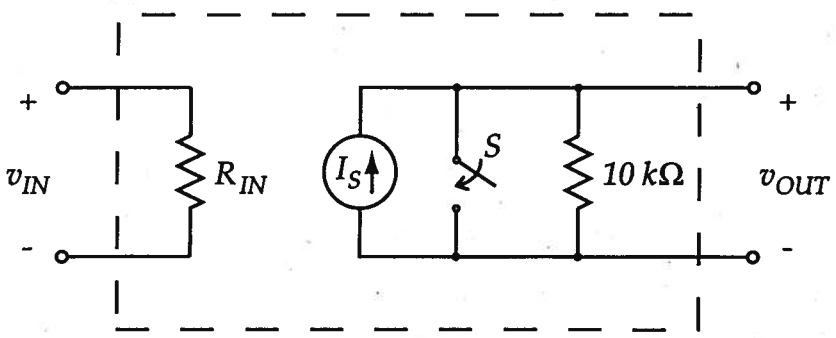


Figure 3: Circuit for Problem 2

Switch S is controlled by the voltage v_{IN} such that it is open when $v_{IN} \leq 1.8V$ and closed otherwise. Also, $I_S = 0.5mA$ in the current source.

(A) Fill in the following table with the output voltages which will result if the circuit is supplied by input voltages which satisfy the digital discipline:

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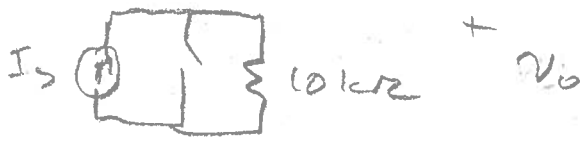
Input	$v_{OUT}(V)$
High	0 V
Low	5 V

$V_{IN} > V_{IH} > V_T$

No current flows through the resistor, so no voltage drop across it. $V_o = 0V$

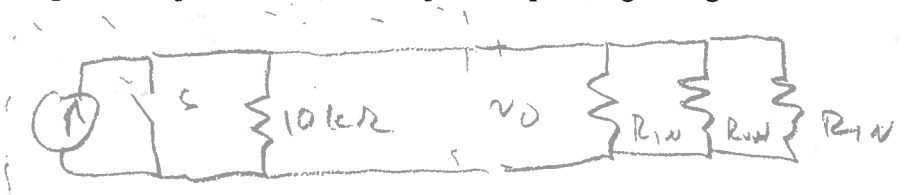
$V_{IN} < V_{IL} < V_T$



$V_o = I_s R = 0.5\,mA \cdot 10k\Omega$

$= 5V$

(B) Each gate in this logic family will have the same input resistance R_{IN}. One of the requirements of this gate is that it be able to drive up to three other gates from this family, connected in parallel. Find the minimum allowable value of R_{IN}, R_{min}, such that this gate will satisfy the digital discipline under all acceptable operating configurations.



If V_{IN} is high the switch is closed; the value of R_{IN} does not matter.
w/ V_{IN} low, the switch is open. The current source is connected to the 10kΩ resistor and 3 R_{IN}s in parallel, so this is an equivalent resistance $R_{eq} = 10k\Omega \| R_{IN}/3 = \frac{10k\Omega \cdot \frac{R_{IN}}{3}}{10k\Omega + \frac{R_{IN}}{3}} = \frac{10k\Omega \cdot R_{IN}}{30k\Omega + R_{IN}}$

We must maintain $V_{out} > V_{OH}$.

$\Rightarrow I_S R_{eq} > V_{OH} \Rightarrow \frac{10k\Omega \cdot R_{min}}{30k\Omega + R_{min}} \cdot 1.5mA = 4V$

$\frac{10k\Omega \cdot R_{min}}{30k\Omega + R_{min}} = 8k\Omega \Rightarrow R_{min} = 120k\Omega$

15

$R_{min} =$ 120 $k\Omega$

(C) What is the noise margin for this logic family (i.e., what is the maximum noise amplitude in V that can appear anywhere in a circuit in which this logic family is used such that all the gates in this circuit are guaranteed to operate properly)?

The noise margins are:

$V_{IL} - V_{OL} = 1.55V - 1.0V = 0.55V$

$V_{OH} - V_{IH} = 4.0V - 3.3V = 0.7V$

The minimum of these is the first: 0.55V

This is the maximum allowable noise amplitude

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Noise margin = 0.55 V

(D) Circle the logic expressions which describe the logic functions implemented by the circuits shown in Figures 4 and 5 from the respective lists below each figure. The circuits employ the logic inverter of Figure 3 (indicated by a rectangular box). You may assume that each MOSFET has threshold voltage, V_T, of $2.0V$.

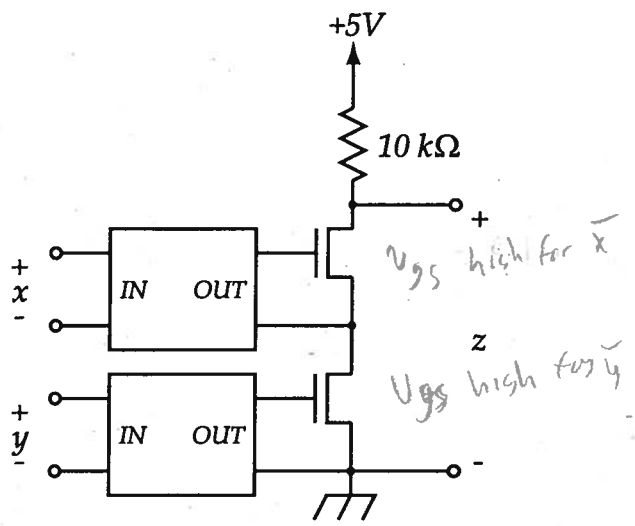


Figure 4: Logic circuit for Problem 2(D)

$z = \overline{xy}$ $\quad z = \bar{x}\bar{y}$ $\quad z = x + y$ $\quad z = \overline{x + y}$

$z = y$ $\quad z = \bar{x} + xy$ $\quad z = \bar{x}y$ $\quad z = x$

$Z = \overline{\bar{x}\,\bar{y}} = x + y$

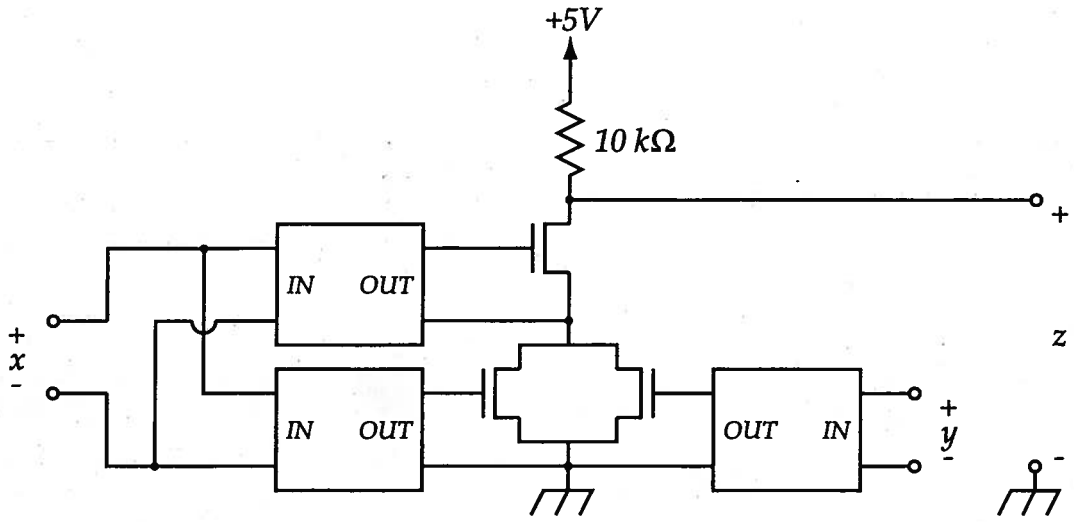
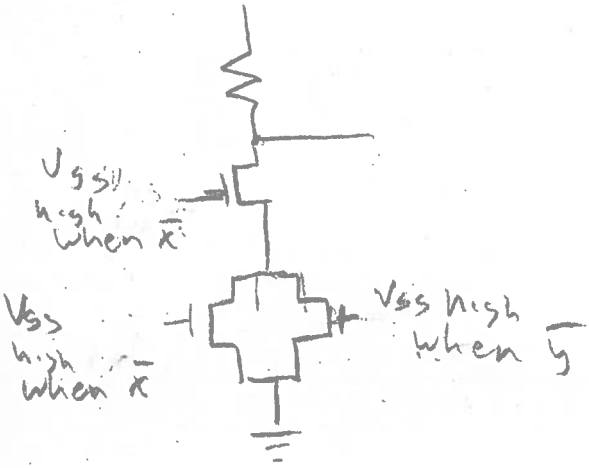
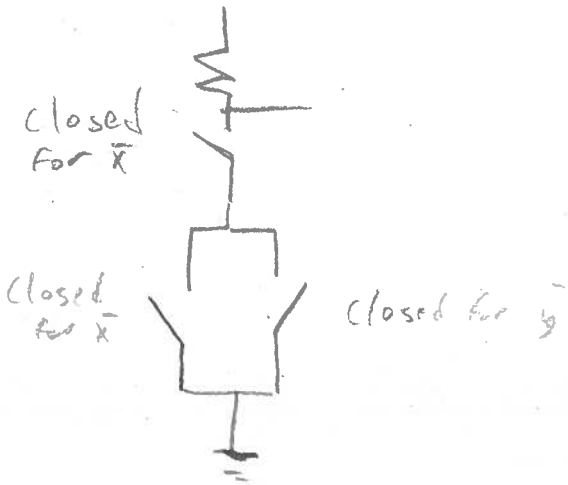


Figure 5: Logic circuit for Problem 2(D)

$z = \overline{xy}$ $z = \bar{x}\bar{y}$ $z = x + y$ $z = \overline{x + y}$

$z = y$ $z = \bar{x} + xy$ $z = \bar{x}y$ $z = x$ (8)





$\bar{Z} = \bar{x} \cdot (\bar{x} + \bar{y})$

$Z = \overline{\bar{x} \cdot (\bar{x} + \bar{y})} = x + \overline{(\bar{x} + \bar{y})} = x + xy = x(1 + y)$

$= x$