

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.004 Computation Structures
Fall 2003

Quiz #1: September 19, 2003

Name	Athena Username	Score
DAN PORTS	drkp	4+9+4+6=23
<input type="checkbox"/> WF 10, 34-304 Morris	<input type="checkbox"/> WF 12, 34-302 Fitzpatrick	<input type="checkbox"/> WF 1, 34-304 Asanovic
<input type="checkbox"/> WF 11, 34-303 Morris	<input checked="" type="checkbox"/> WF 12, 34-303 Mazzola Paluska	<input type="checkbox"/> WF 2, 34-303 Asanovic
<input type="checkbox"/> WF 11, 36-372 Fitzpatrick	<input type="checkbox"/> WF 1, 34-303 Mazzola Paluska	

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Problem 1. (4 points): Warmup

(A) Is it possible to design a combinational inverter whose contamination delay exceeds its propagation delay?

Circle one: YES

NO

(B) Is a conventional two-input CMOS NAND gate, constructed as shown in lecture, *lenient*?

Circle one:

YES

NO

(C) In Lecture 4, you saw that a 2^k -input XOR could be implemented as a k -level tree of 2-input gates. Can *every* 2^k -input, 1-output combinational function be implemented as a k -level tree of (not necessarily identical) 2-input 1-output gates?

Circle one: YES

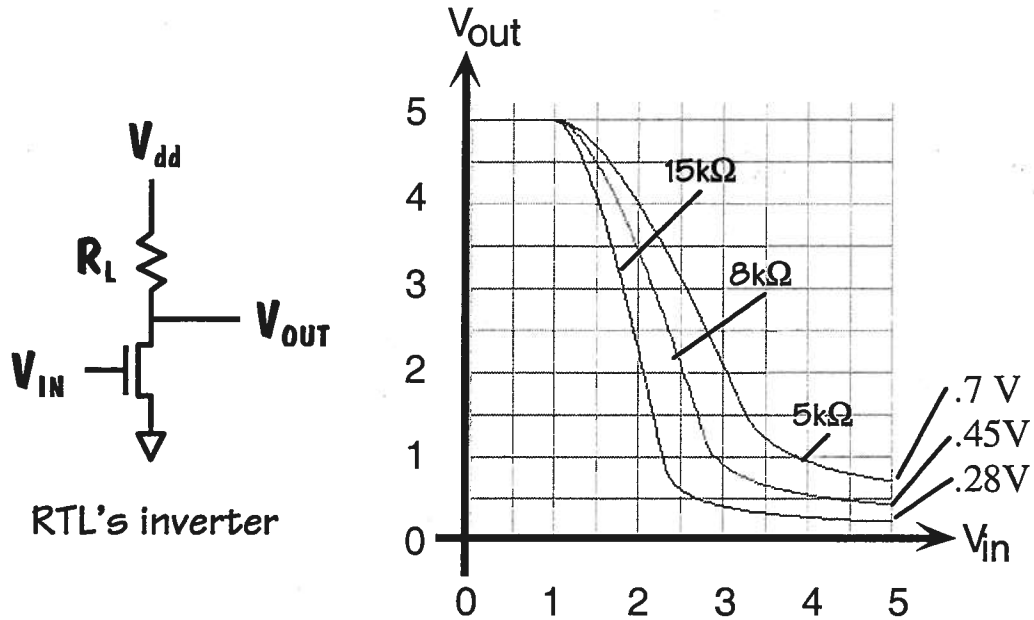
NO

(D) You are trying to determine the registration number on Alice's Belize license plate. You know that license plates in Belize have four characters, each either a digit or an upper-case letter, and are selected randomly consistently with this format. Alice tells you that the license plate in question contains only digits. How much information has Alice given you about her license plate?

Give an expression for the amount of information in the message:

$$\log_2 \left(\frac{36^4}{10^4} \right) = 4 \log_2 \left(\frac{36}{10} \right)$$

Problem 2. (9 points) Really Terrific Logic, anticipating a global shortage of holes, has introduced a line of logic devices built using only n-channel mosfets and resistors (no pfets!). RTL's inverter device is shown below. On the right is a diagram showing the inverter's voltage transfer curve for three possible choices for resistance of the pullup resistor (R_L).



(A) (1 point) Which choice for R_L will provide the inverter with the fastest output rise time?

R_L that gives the fastest output rise time (one of $15k\Omega$, $8k\Omega$, $5k\Omega$): $5k\Omega$

(B) (4 points) RTL engineers have chosen $R_L = 8k\Omega$ and proposed four sets of values for the input/output voltage specifications of the RTL inverter. Using the voltage transfer curve, for each set of values circle "VALID" if the proposed values would yield a valid combinational device, otherwise circle "INVALID." If you need them, scratch copies of the VTC can be found at the end of the quiz.

$V_{OL} = 0.5V$, $V_{IL} = 1.0V$, $V_{IH} = 3.5V$, $V_{OH} = 4.0V$: (circle one) VALID INVALID

$V_{OL} = 1.0V$, $V_{IL} = 1.5V$, $V_{IH} = 3.5V$, $V_{OH} = 4.0V$: (circle one) VALID INVALID

$V_{OL} = 1.0V$, $V_{IL} = 1.5V$, $V_{IH} = 4.5V$, $V_{OH} = 5.0V$: (circle one) VALID INVALID

$V_{OL} = 1.0V$, $V_{IL} = 2.0V$, $V_{IH} = 3.0V$, $V_{OH} = 3.1V$: (circle one) VALID INVALID

One of the main selling points of CMOS technology is its extremely low static power dissipation. RTL is a bit nervous about the static power dissipation of their devices and asks you to consider a benchmark circuit consisting of 1,000,000 inverters connected in a series chain. Assume, in the following, that voltage parameters have been chosen to make the inverter a valid combinational device.

(C) (1 point) Suppose the input to the first inverter in the chain is a logical 0. What is the logical output of the last (millionth) inverter in the chain?

Logical output of last inverter in chain, given input 0: 0

(D) (2 points) Give the approximate static power dissipation of the 1,000,000 RTL inverters connected in a series chain. Assume that $R_L = 8k\Omega$, $V_{DD} = 5V$ and that the FET source-drain resistance is $2k\Omega$ when "on" and infinite when "off".

$\frac{V^2}{R} = \frac{(5V)^2}{10k\Omega} = \frac{25}{10000} = 2.5 \times 10^{-3} W$ (per inverter)
 Power dissipation for chain of 1,000,000 RTL inverters (watts): 1250 W

(E) (1 point) Estimate the static power dissipation of a chain of 1,000,000 CMOS inverters under similar assumptions (each NFET and PFET has $2k\Omega$ "on" resistance, infinite "off" resistance).

Power dissipation for chain of 1,000,000 CMOS inverters (watts): 0

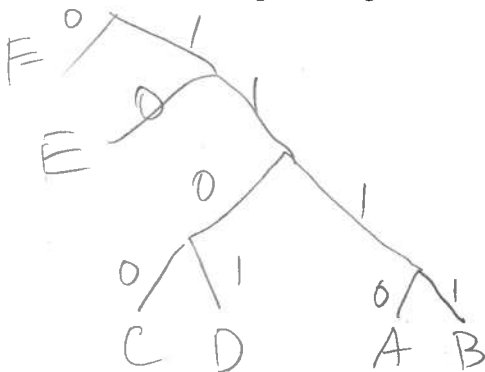
4 **Problem 3. (4 points): Variable length Encoding**

The dwindling population of a 60s-era cult is trying to rejuvenate their membership via a wireless PDA that emphasizes the cult's peculiar values. You've been asked to help, by coming up with a variable-length Huffman encoding that conveys one of the following tidbits about today's date. Assume that only one of the descriptions applies to each date.

AB $5/365$
 CD $8/365$
 ABCD $13/365$

- A: If today is an equinox (there are 2 of these per year); $2/365$
- B: If today is the birthday of one of the cult's three saints: Thelonius Monk, Victor Hugo, or Tiny Tim (there are 3 of these per year); $3/365$
- C: If today is the first day of a new season (there are 4 of these per year); $4/365$
- D: If today is the first day of a month whose name does not contain an 'R' (there are 4 of these per year); $4/365$
- E: If today is a weekend (there are about 100 of these per year); and $100/365$
- F: Otherwise (i.e., a weekday other than the above special cases). $365 - 13 = 252$

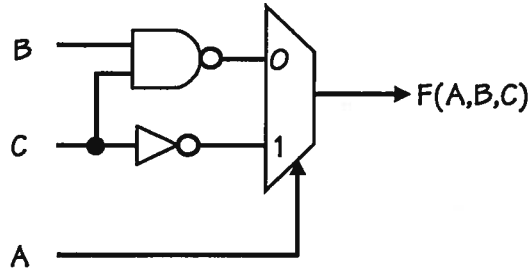
Devise a variable-length Huffman code which encodes the above six messages with the minimum average message size



- Encoding for message A: 1110
- Encoding for message B: 1111
- Encoding for message C: 1100
- Encoding for message D: 1101
- Encoding for message E: 10
- Encoding for message F: 0

6 **Problem 4. (8 points)**

Consider the following circuit that implements the 3-input function $F(A,B,C)$:



The timing specifications of the components are summarized below:

Component	t_{PD}	t_{CD}
Multiplexor	7 ns	2 ns
NAND	5 ns	1 ns
Inverter	1 ns	0

A	B	C	$F(A,B,C)$
0	0	0	1 ✓
0	0	1	1 ✓
0	1	0	1 ✓
0	1	1	0 ✓
1	0	0	1 ✓
1	0	1	0 ✓
1	1	0	1 ✓
1	1	1	0 ✓

(A) (2 points) Give appropriate propagation and contamination delay specifications for this circuit.

Propagation delay: 12 ns ✓

Contamination delay: 2 ns ✓

(B) (4 points) Fill in the truth table to the left.

(C) (2 points) Can the function $F(A, B, C)$ be implemented as a single 3-input CMOS gate consisting of an output node connected to complementary pullup and pulldown circuits? If so, give the minimum number of transistors (NFETS and PFETS) required to implement the gate. Enter "NONE" if no such gate exists.

Enter transistor count or "NONE": NONE ^{x-2}
END OF QUIZ!