

MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.004 Computation Structures  
Fall 2003

Quiz #2: October 10, 2003

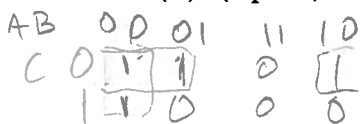


Name	Athena Username	Score
DAN PORTS	drkp	7+9+4+5=
<input type="checkbox"/> WF 10, 34-304 Morris	<input type="checkbox"/> WF 12, 34-302 Fitzpatrick	<input type="checkbox"/> WF 1, 34-304 Asanovic
<input type="checkbox"/> WF 11, 34-303 Morris	<input checked="" type="checkbox"/> WF 12, 34-303 Mazzola Paluska	<input type="checkbox"/> WF 2, 34-303 Asanovic
<input type="checkbox"/> WF 11, 36-372 Fitzpatrick	<input type="checkbox"/> WF 1, 34-303 Mazzola Paluska	

25!!!  
YAY!!!

**Problem 1:** (7 points) The minority function  $m(A,B,C)$  of three inputs is 1 if no more than one of the three inputs is 1, otherwise it's 0.

(A) (1 point) Give a minimal sum-of-products expression for  $m(A,B,C)$ :

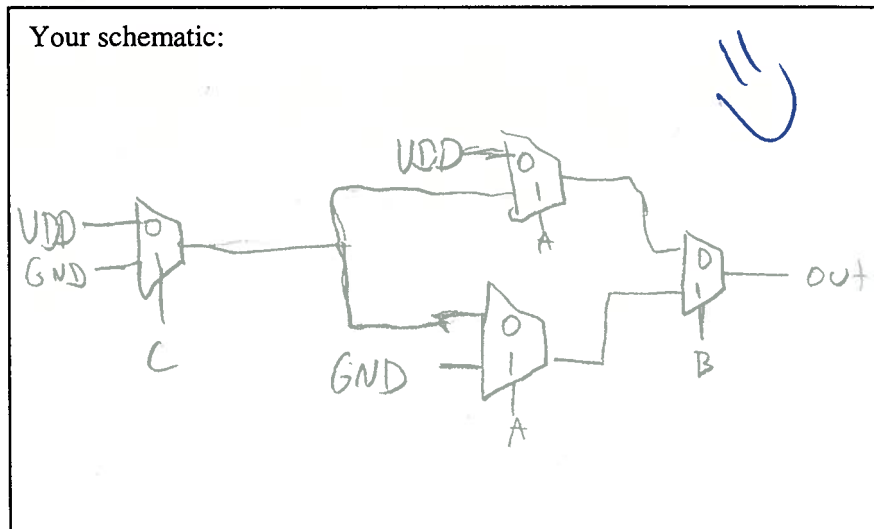
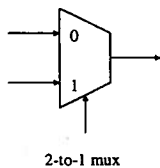


$$\bar{A}\bar{C} + \bar{B}\bar{C} + \bar{A}\bar{B}$$

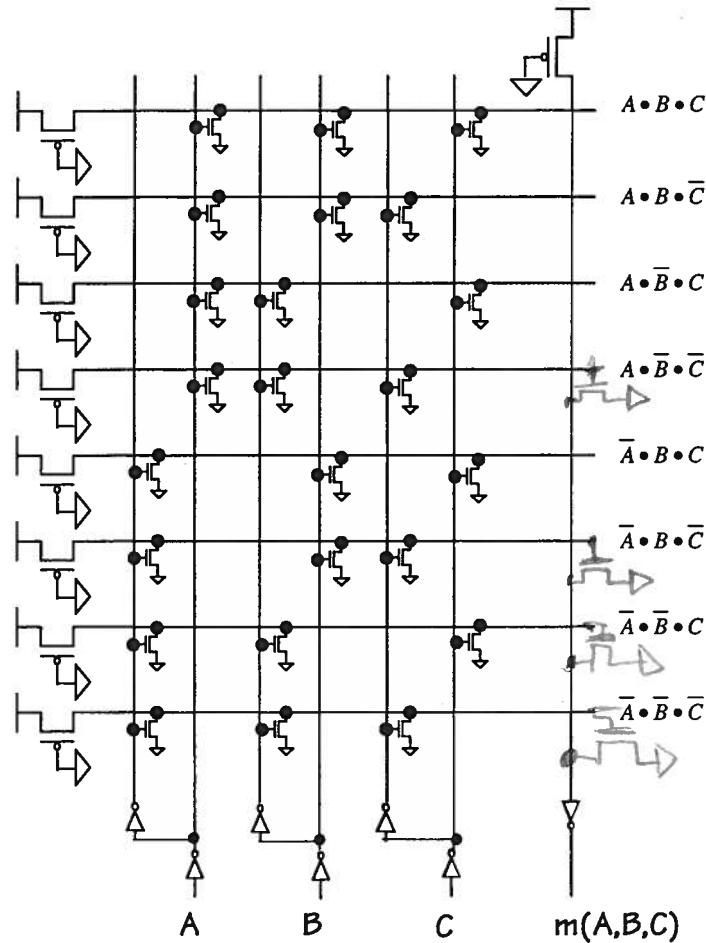
Minimal sum-of-products expression:  $\bar{A}\bar{C} + \bar{B}\bar{C} + \bar{A}\bar{B}$

3

(B) (3 points) You want to build a combinational circuit that implements  $m(A,B,C)$  but when you go to Instrument Desk all they have are 2-to-1 multiplexers. Give a circuit diagram that implements  $m$  using just multiplexers and connections to  $A$ ,  $B$ ,  $C$ ,  $VDD$  (for a logic "1") and  $GND$  (for a logic "0"). Please use the schematic symbol shown below when drawing your schematic.

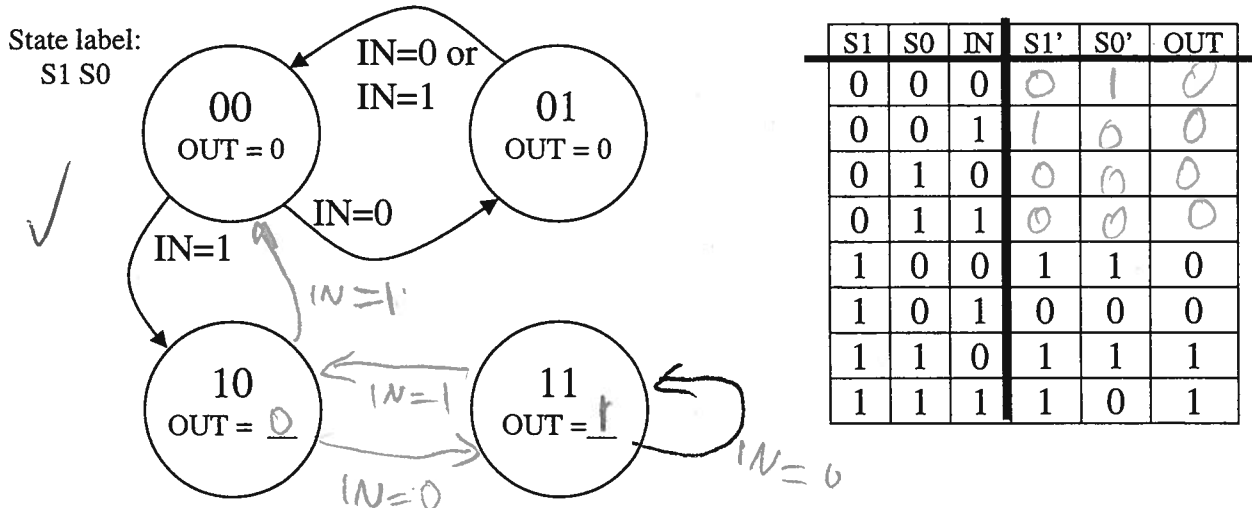


(C) (3 points) The following ROM can be used to implement any 3-input Boolean function. Please fill in the appropriate mosfets to complete the implementation of  $m(A,B,C)$ :



9 **Problem 2: (9 points) FSM**

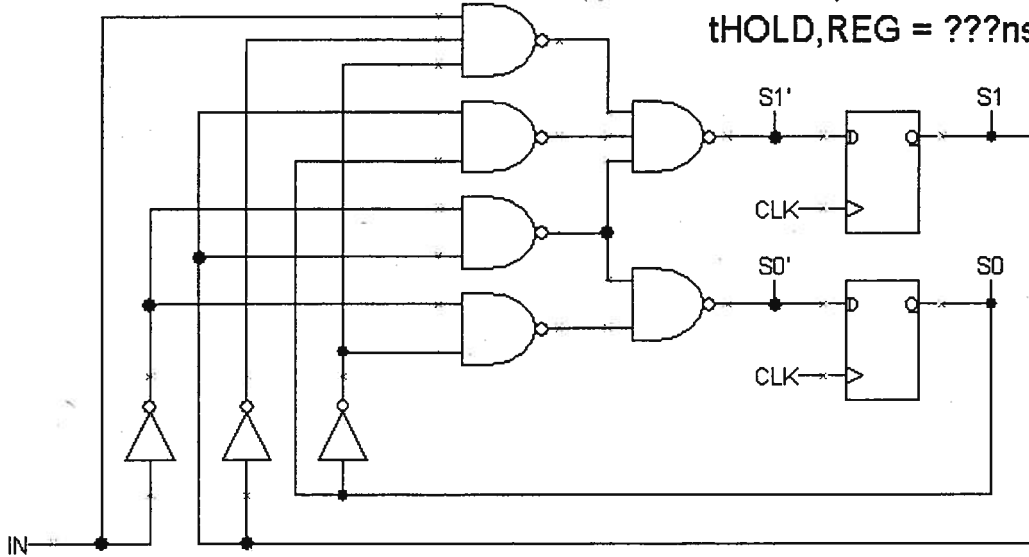
45 (A) (5 points) The following state transition diagram and truth table document the same finite state machine. Please fill in the missing entries in both the diagram and table. Remember to specify the value of OUT for each state in the diagram.



The following circuit diagram implements the FSM shown above:

$t_{CD, LOGIC} = 2ns$   
 $t_{PD, LOGIC} = 9ns$

$t_{CD, GATES} = 1ns$  for each NAND / INV  
 $t_{PD, GATES} = 3ns$   
 $t_{CD, REG} = 2ns$   
 $t_{PD, REG} = 4ns$   
 $t_{SETUP, REG} = 2ns$   
 $t_{HOLD, REG} = ???ns$



- (B) (1 point) What's the largest that the register's hold time ( $t_{HOLD,REG}$ ) can be if the circuit is to work correctly? Write "NONE" if there is no constraint on  $t_{HOLD,REG}$  or if it cannot be determined from the information provided.

$t_{PD,REG} + 2 \cdot t_{PD,GATES} = 4 + 2 = 4ns$

$t_{HOLD,REG}$  must be less than or equal to: 4 ns ✓

- (C) (1 point) What's the smallest that the clock period can be if the circuit is to work correctly? Write "NONE" if there is no constraint on the clock period or if it cannot be determined from the information provided.

$t_{PD,REG} + 3 \cdot t_{PD,GATES} + t_{SETUP,REG} = 4 + 3 \cdot 3 + 2 = 15ns$

$t_{CLK}$  must be greater than or equal to: 15 ns ✓

- (D) (2 points) Specify setup and hold times for IN with respect to the rising edge of CLK if the circuit is to work correctly. For this question assume that  $t_{HOLD,REG} = 3ns$ . Write "NONE" if there are no constraints on the value or if it cannot be determined from the information provided.

$t_{S,IN} = t_{SETUP,REG} + 3 \cdot t_{PD,GATES}$   
 $= 2ns + 3 \cdot 3ns = 11ns$

$t_{SETUP,IN}$ : 11 ns ✓

$t_{H,IN} = t_{HOLD,REG} - 2 \cdot t_{CD,GATES}$   
 $= 3ns - 2 \cdot 1ns = 1ns$

$t_{HOLD,IN}$ : 1 ns ✓

**Problem 3.** (4 points) For each of the following circuits indicate whether or not it can be built to perform the specified function in bounded time with 100% reliability. You may assume that the components and connections used to build the circuits are built are 100% reliable, i.e., we are only asking if the circuits may fail to meet their specification because of inescapable metastability issues. Each circuit has two inputs, A and B, which are connected to buttons controlled by game show contestants. An input reliably makes a single transition from 0 to 1 when a contestant presses the corresponding button.

- (A) (1 point) A circuit that determines if button A was pressed before a specified deadline (button B is ignored). Assume the circuit has an accurate internal signal that transitions from 0 to 1 when the deadline is reached. The output should be 1 if the button was pressed on or before the deadline, 0 if pressed after the deadline. The output should be valid and stable within a specified  $t_{PD}$  of the A input transition.

Can build (circle one): YES  NO

- (B) (1 point) A circuit that determines if at least one contestant has pressed his/her button. The output should be 1 if at least one button has been pressed, 0 otherwise. The output should be valid and stable within a specified  $t_{PD}$  of the first input transition.

Can build (circle one):  YES NO

- (C) (1 point) A circuit that determines which of two game show contestants pressed their button *second*. The output should be 0 if A pressed her button second, and 1 if contestant B pressed his button second. If the two presses happened with  $t_E$  seconds, the circuit is allowed to output either a 0 or a 1 (but must output a valid value). The output should be valid and stable within a specified  $t_{PD}$  of the second input transition.

Can build (circle one): YES  NO

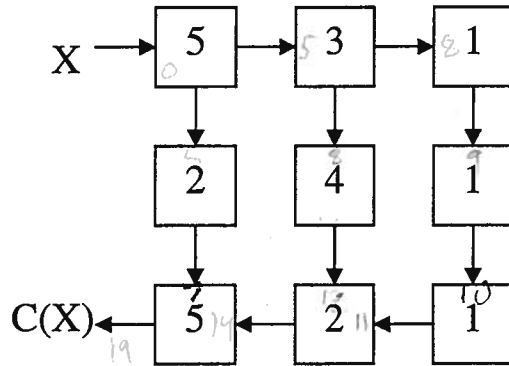
- (D) (1 point) Suppose there are two output signals encoded as follows:

00 no output is available  
01 contestant A wins  
10 contestant B wins  
11 if the circuit has decided there was a "tie"

If we wished to rig the results, can we build a circuit that waits until both contestants have pressed their buttons and then signals "01" (i.e., A wins) independent of the of the actual order in which the buttons were pressed? The outputs should be valid and stable within a specified  $t_{PD}$  of the most recent input transition.

Can build (circle one):  YES NO

**Problem 4:** (5 points) The National Security Agency has designed a new encryption device called the Conundrum, composed of nine combinational modules connected as shown in the diagram below:



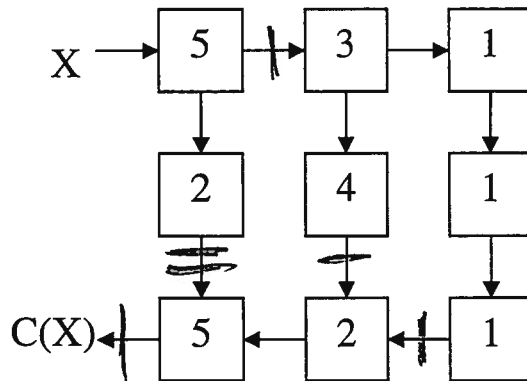
The device takes an integer value  $X$  and computes an encrypted version  $C(X)$ . In the diagram above each combinational component is marked with its propagation delay in microseconds; contamination delays are zero for each component.

(A) (1 point) What is the latency and throughput of the Conundrum device?

Latency (microseconds): 19  $\mu$ s

Throughput (1/microseconds): 1/19  $\mu$ s

3 (B) (3 points) The NSA needs to produce a version of the Conundrum device that has a throughput greater than or equal to  $1/(7\mu\text{s})$  but wants the implementation with the smallest latency that meets the throughput constraint. Using the diagram below indicate the locations for ideal (zero-delay) registers to create a pipelined implementation that meets these goals. Remember that your answer should have a register on the output signal.



Extra copies of this diagram can be found on the following page.

(C) (1 point) What is the latency and throughput of your pipelined implementation?

Latency (microseconds): 21  $\mu$ s Throughput (1/microseconds): 1/7  $\mu$ s

