6.111 **Dan Ports**

Lab 1

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Part I — TTL Static Electrical Characteristics:

An inverter was created using a NAND gate on a 74LS00 as drawn in Figure 4 of the lab handout. Output values were measured using the oscilloscope. With the input high, the inverter produced a low output value of 60 mV. With the input low, the inverter produced a high output value of 4.7 V.

Part II — TTL Dynamic Electrical Characteristics:

A ring oscillator was wired using five TTL inverters on a 74LS04. The voltage was measured relative to ground at the input to one of the inverters using the oscilloscope. A waveform sketch is attached. The measured period of oscillation was 53.6 ns. To complete one full period, the signal must travel through five inverters twice: once to invert the original signal, and once to bring it back to its original state. Thus, the average propagation delay of an inverter was 5.36 ns.

One of the short wire connections in the ring oscillator was removed and replaced with a much longer wire. The period of oscillation increased to 89 ns due to increased propagation delay through the wire.

Part III — Flip-Flop Operation Times:

A 74LS393 8-bit ripple counter was wired to a 1.8432 MHz crystal oscillator as in Figure 8 in the lab handout. To determine the operation time of a flip flop, the clock input and most significant output bit (2D, pin 8) were measured with an oscilloscope. The scope was triggered on a rising edge of the most significant bit. A waveform sketch is attached. A delay of 98 ns was measured between the falling edge of the clock and the rising edge of the MSB output. There are 8 flip flops in the ripple counter, and they are triggered in sequence in this transition, so the average operation time for a flipflop in the ripple counter is $\frac{98}{8}$ ns = 12.25 ns.

Part IV — Timing Analyzer Operation:

The CLK, Q1B, and Q2D signals from the 393 ripple counter were connected to inputs on the logic analyzer with TTL threshold and positive polarity. Waveform sketches are attached. The timing analyzer was triggered on a falling edge of Q2D. The delay time from a falling edge of the CLK signal to a falling edge of Q2D was measured as 104 ns.

The ring oscillator was connected to the RING signal on the timing analyzer. The analyzer was triggered on a rising edge of RING. The period of the signal was measured as 56 ns.

A glitchy output was generated by connecting a sequence of 74LS00 NAND gates to the Q2D output of the ripple counter, as drawn in Figure 9 of the lab handout. The output of this circuit was connected to the /GLIT signal on the logic analyzer, and the analyzer was triggered on a falling edge of this signal. The width of the glitch was measured as 12 ns.

Part V — Counter:

Two 74LS163 4-bit TTL counters were wired in an always-counting configuration, as drawn in Figure 11. The clock signal was connected to the Q2A output of the 74LS393 ripple counter. The oscilloscope was connected to the LS163's clock input and least significant output bit, and triggered on a rising edge of the LSB output. The time between a rising edge of the clock and a rising edge of the LSB was measured to be 20 ns. This is the operation delay of one flipflop in the LS163. No glitches were observed on the carry output with a logic analyzer configured in glitch mode.

Part VI — Programming a 20V8:

The 20V8 PAL was programmed with the provided VHDL file. A logic diagram for the latch and square root statements in the VHDL source file is attached.

Part VII — Analyze and Test the Latch:

A logic diagram using AND and NOR gates that implements the latch in the last two statements in the VHDL source is attached. The latch circuit was also implemented in SSI using NAND gates: two 74LS00 chips and one 74LS10. A logic diagram is attached. One set of four switches was connected to the LATCHCLK, DATA, SET, and RESET signals of both the PAL and SSI latch implementations. LEDs were connected to the QH and QL outputs of each implementation. The latch was then tested. Both the PAL and SSI implementation gave identical results.

With LATCHCLK set low, setting S high and R low causes QH to become high and QL to become low. Setting R high and S low causes QH to become low and QL to become high. With S, R, and LATCHCLK set low, the state of QH and QL stays constant, regarldess of the setting of DATA. With S and R set low and LATCHCLK set high, the value of QH is equal to that of the DATA input, and QL is its complement. If the DATA input is wired to the complement of the QH output, the latch will continue to behave the same way when LATCHCLK is low, but will oscillate when LATCHCLK is high.

Part VIII — Analyze and Test Your Combinatorial Logic:

Five counter outputs from the 74LS163 counters were connected to the A0 through A4 inputs on the PAL, as depicted in Figure 11 in the lab handout. The A0 through A4 inputs and X0, X1, and X2 outputs were connected to the logic analyzer, configured in timing mode and triggered on a falling edge of the A4 signal. The outputs X0-X2 correctly give the square root of the input A. A waveform sketch is attached.

Using the logic analyzer in glitch mode, glitches were observed in X0 when the input transitions from the 7 to 8 state, and from 23 to 24. These correspond to a static hazard in the combinatorial logic for the X0 output.

With the timing analyzer triggered on the falling edge of A4, the time until a transition in the output signals was measured to determine the combinatorial logic delay. This delay was 8.0 ns.

Part IX — Analyze and Test the T, D, and JK Flip Flops:

The D, T, J and K signals of the flip flops implemented in the PAL were wired to the Q1, Q2, Q3, and Q4 outputs of the LS163 counter respectively, and the FFCLK signal was connected to the clock signal driving the LS163. The same three flip flops were implemented in SSI using two 74LS74 flipflops and two 74LS00 quad NAND gates, and connected to the same input signals. A logic diagram is attached.

The inputs and outputs to each flip flop were connected to the analyzer, and triggered off the falling edge of the K signal (which had the longest period). The output from the PAL and SSI flip flops were identical. A sketch of the output is attached. The flip flops operated correctly: the D flip flop captured the state of the D input on a rising edge of the clock. The T flip flop toggled its output value when the T input was high on the rising edge of the clock and maintained its state when T was low. On the rising edge of the clock, the JK flip flop set its output high when J was high and K was low, set its output low when K was high and J was low, toggled its output when J and K were both high, and maintained state when J and K were both low.

The analyzer was then triggered on the rising edge of the D output. The time between the rising edge of FFCLK and the rising edge of D was measured in order to determine the operating time of a flip flop. This was performed for both the PAL and SSI flipflops. The operating time was measured as 16 ns for the 74LS74 and 8 ns for the PAL.

Part X — Logic Analyzer as as State Analyzer:

The logic analyzer was configured as a state analyzer. The four-bit A input and the three bit X output to the square-rooter, the D, T, J, and K inputs and DFF, TFF, and JKFF outputs to the flipflops were connected to the analyzer, and the CLK signal was used as the analyzer clock.

A printout of the state analyzer output is attached. The square rooter and flipflops give the correct output.