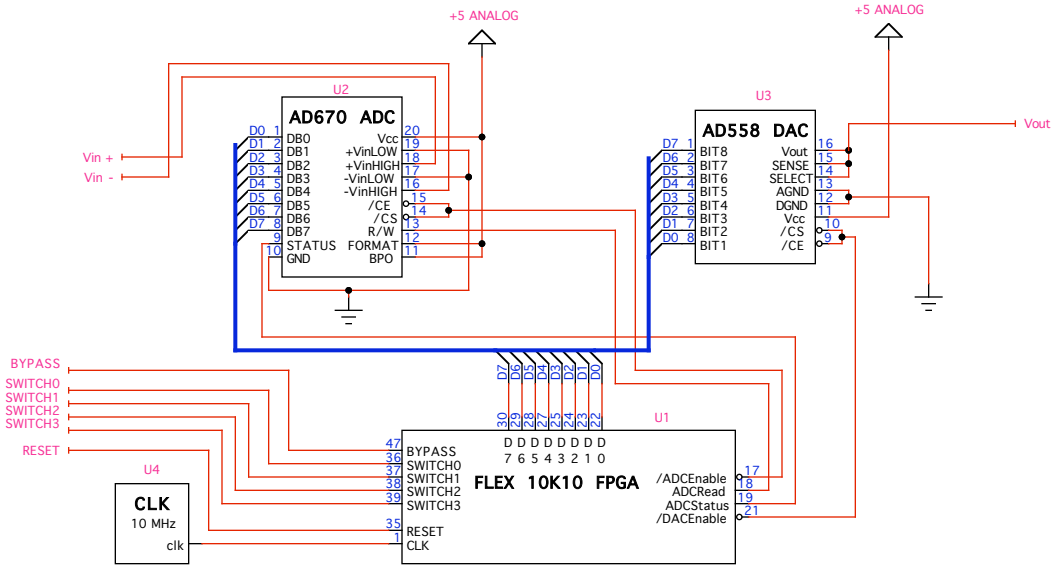
+5 ANALOG
+5 ANALOG
U2
AD670 ADC
D0 1 DB0
D1 2 DB1
D2 3 DB2
D3 4 DB3
D4 5 DB4
D5 6 DB5
D6 7 DB6
D7 8 DB7
9 STATUS
10 GND
Vcc 20
+VinLOW 19
+VinHIGH 18
-VinLOW 17
-VinHIGH 16
/CE 15
/CS 14
R/W 13
FORMAT 12
BPO 11
Vin +
Vin -
U3
AD558 DAC
D7 1 BIT8
D6 2 BIT7
D5 3 BIT6
D4 4 BIT5
D3 5 BIT4
D2 6 BIT3
D1 7 BIT2
D0 8 BIT1
Vout 16
SENSE 15
SELECT 14
AGND 13
DGND 12
Vcc 11
/CS 10
/CE 9
Vout
BYPASS
SWITCH0
SWITCH1
SWITCH2
SWITCH3
RESET
D7 D6 D5 D4 D3 D2 D1 D0
30 29 28 27 25 24 23 22
U1
D D D D D D D D
7 6 5 4 3 2 1 0
FLEX 10K10 FPGA
47 BYPASS
36 SWITCH0
37 SWITCH1
38 SWITCH2
39 SWITCH3
35 RESET
1 CLK
/ADCEnable 17
ADCRead 18
ADCStatus 19
/DACEnable 21
U4
CLK
10 MHz
clk