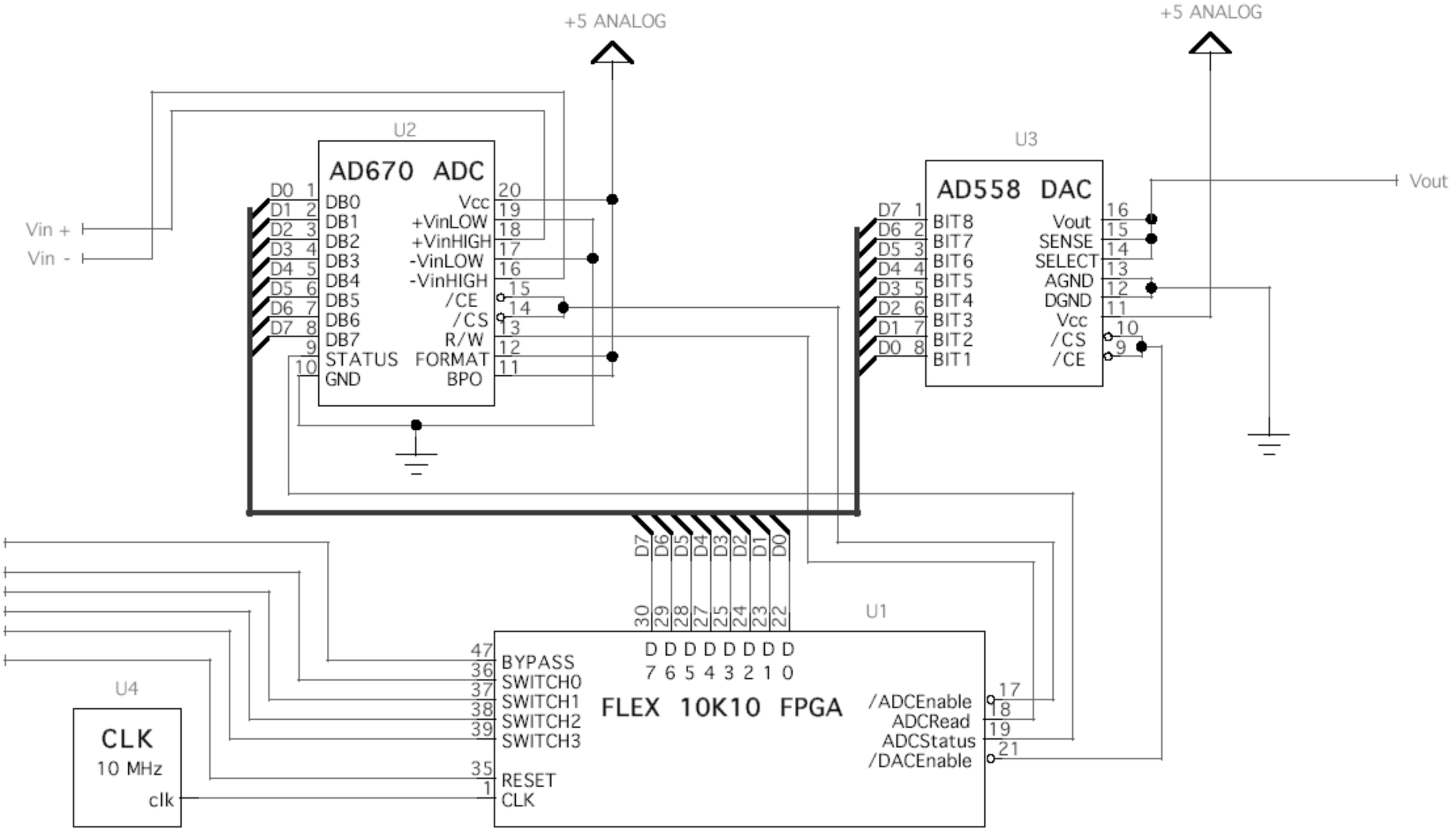
+5 ANALOG
U2
AD670 ADC
D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
D7 8
9
10
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
STATUS
GND
Vcc 20
+VinLOW 19
+VinHIGH 18
-VinLOW 17
-VinHIGH 16
/CE 15
/CS 14
R/W 13
FORMAT 12
BPO 11
Vin +
Vin -
+5 ANALOG
U3
AD558 DAC
D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
BIT8
BIT7
BIT6
BIT5
BIT4
BIT3
BIT2
BIT1
Vout 16
SENSE 15
SELECT 14
AGND 13
DGND 12
Vcc 11
/CS 10
/CE 9
Vout
BYPASS
SWITCH0
SWITCH1
SWITCH2
SWITCH3
RESET
D7 D6 D5 D4 D3 D2 D1 D0
30 29 28 27 25 24 23 22
U1
D D D D D D D D
7 6 5 4 3 2 1 0
47 BYPASS
36 SWITCH0
37 SWITCH1
38 SWITCH2
39 SWITCH3
35 RESET
1 CLK
FLEX 10K10 FPGA
/ADCEnable 17
ADCRead 18
ADCStatus 19
/DACEnable 21
U4
CLK
10 MHz
clk