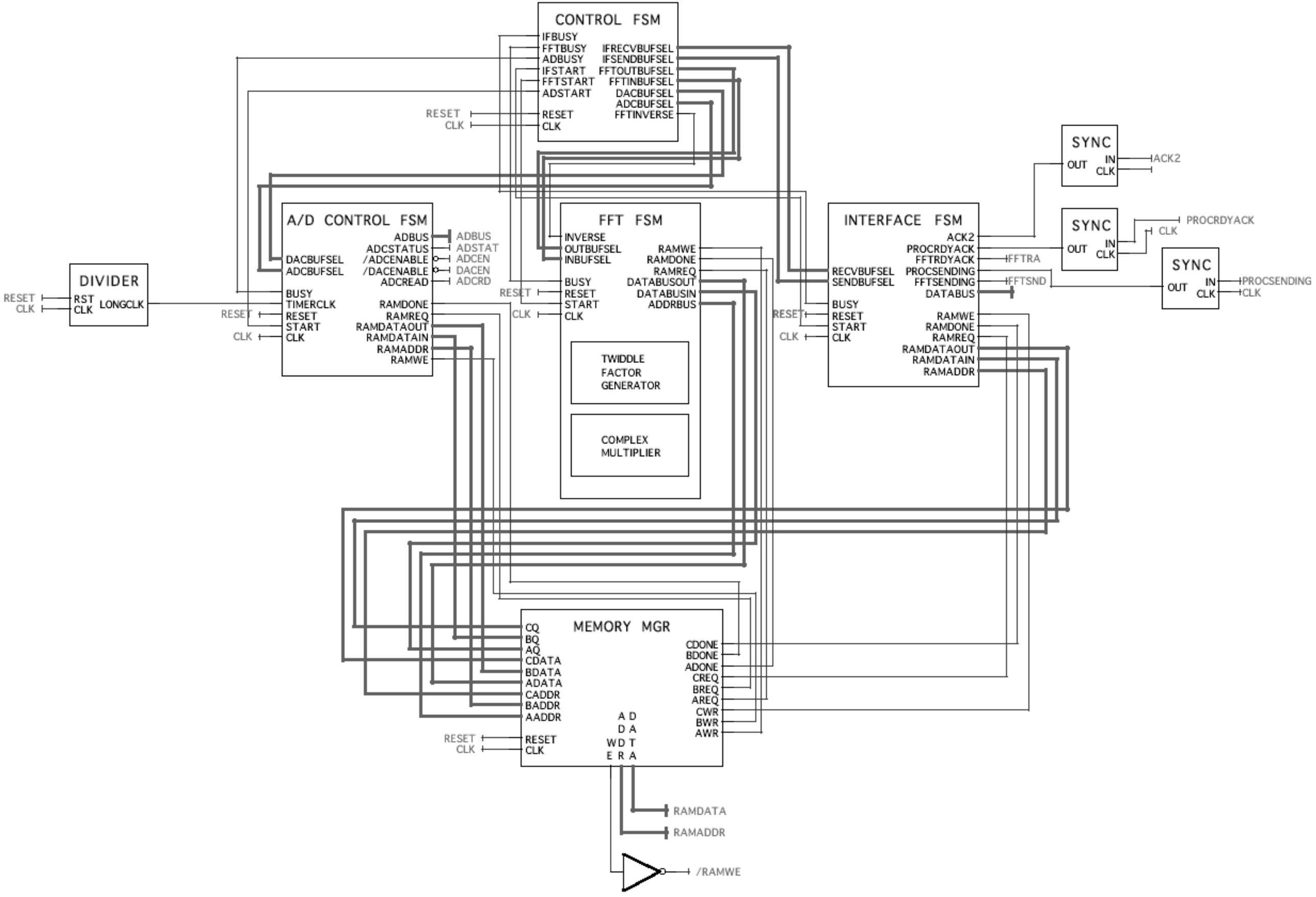
CONTROL FSM
IFBUSY
FFTBUSY
ADBUSY
IFSTART
FFTSTART
ADSTART
RESET
CLK
IFRECVBUFSEL
IFSENDBUFSEL
FFTOUTBUFSEL
FFTINBUFSEL
DACBUFSEL
ADCBUFSEL
FFTINVERSE
DIVIDER
RST
CLK
LONGCLK
A/D CONTROL FSM
DACBUFSEL
ADCBUFSEL
BUSY
TIMERCLK
RESET
START
CLK
ADBUS
ADCSTATUS
/ADCENABLE
/DACENABLE
ADCREAD
RAMDONE
RAMREQ
RAMDATAOUT
RAMDATAIN
RAMADDR
RAMWE
FFT FSM
INVERSE
OUTBUFSEL
INBUFSEL
BUSY
RESET
START
CLK
RAMWE
RAMDONE
RAMREQ
DATABUSOUT
DATABUSIN
ADDRBUS
TWIDDLE FACTOR GENERATOR
COMPLEX MULTIPLIER
INTERFACE FSM
RECVBUFSEL
SENDBUFSEL
BUSY
RESET
START
CLK
ACK2
PROCRDYACK
FFTRDYACK
PROCSENDING
FFTSENDING
DATABUS
RAMWE
RAMDONE
RAMREQ
RAMDATAOUT
RAMDATAIN
RAMADDR
SYNC
OUT
IN
CLK
ACK2
SYNC
PROCRDYACK
SYNC
PROCSENDING
MEMORY MGR
CQ
BQ
AQ
CDATA
BDATA
ADATA
CADDR
BADDR
AADDR
RESET
CLK
CDONE
BDONE
ADONE
CREQ
BREQ
AREQ
CWR
BWR
AWR
A D
D A
WD T
E R A
RAMDATA
RAMADDR
/RAMWE