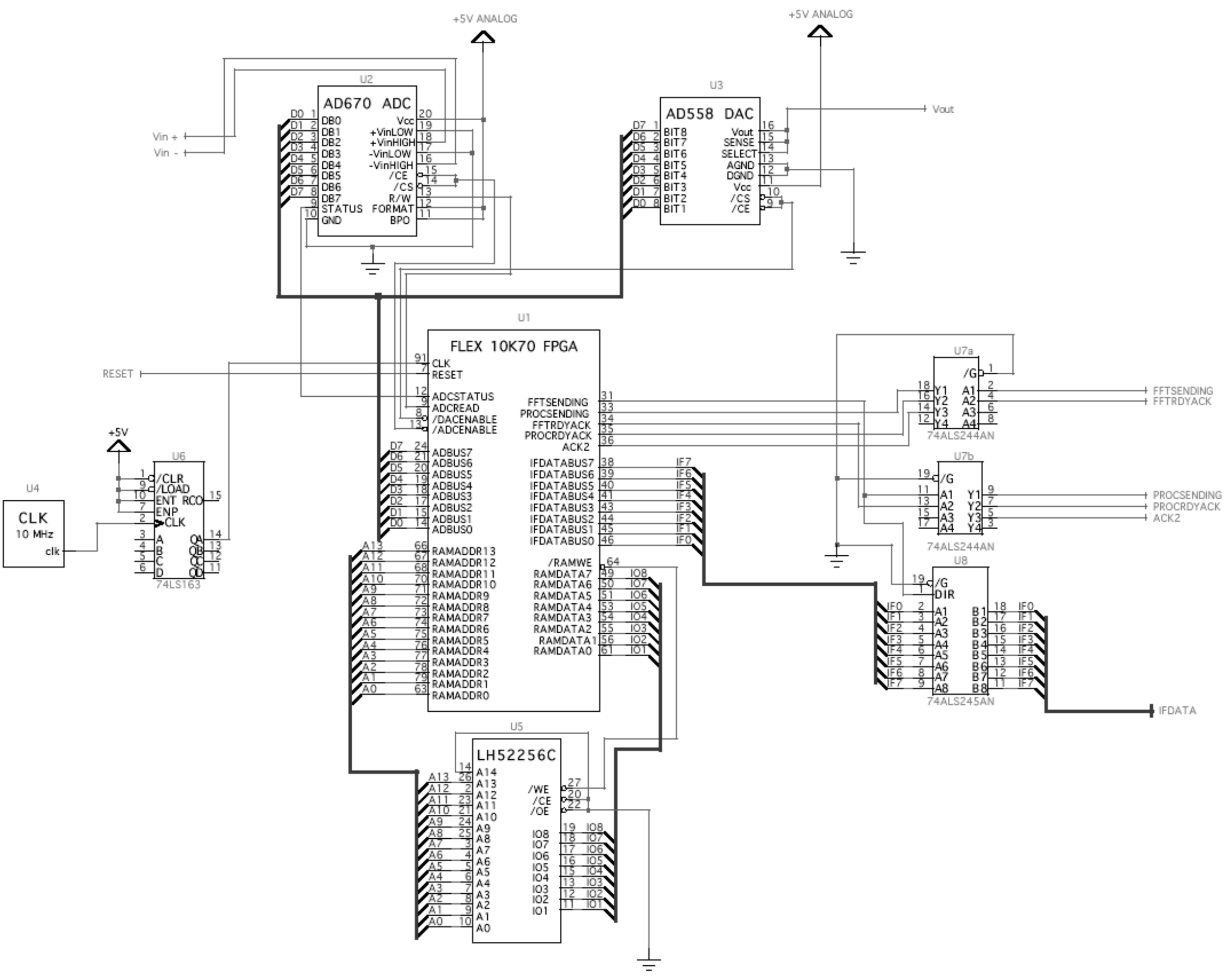
+5V ANALOG
+5V ANALOG
U2
AD670 ADC
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
STATUS
GND
Vcc
+VinLOW
+VinHIGH
-VinLOW
-VinHIGH
/CE
/CS
R/W
FORMAT
BPO
Vin +
Vin -
U3
AD558 DAC
BIT8
BIT7
BIT6
BIT5
BIT4
BIT3
BIT2
BIT1
Vout
SENSE
SELECT
AGND
DGND
Vcc
/CS
/CE
Vout
U1
FLEX 10K70 FPGA
CLK
RESET
ADCSTATUS
ADCREAD
/DACENABLE
/ADCENABLE
ADBUS7
ADBUS6
ADBUS5
ADBUS4
ADBUS3
ADBUS2
ADBUS1
ADBUS0
RAMADDR13
RAMADDR12
RAMADDR11
RAMADDR10
RAMADDR9
RAMADDR8
RAMADDR7
RAMADDR6
RAMADDR5
RAMADDR4
RAMADDR3
RAMADDR2
RAMADDR1
RAMADDR0
FFTSENDING
PROCSENDING
FFTRDYACK
PROCRDYACK
ACK2
IFDATABUS7
IFDATABUS6
IFDATABUS5
IFDATABUS4
IFDATABUS3
IFDATABUS2
IFDATABUS1
IFDATABUS0
/RAMWE
RAMDATA7
RAMDATA6
RAMDATA5
RAMDATA4
RAMDATA3
RAMDATA2
RAMDATA1
RAMDATA0
RESET
+5V
U4
CLK
10 MHz
clk
U6
/CLR
/LOAD
ENT RCO
ENP
CLK
74LS163
U5
LH52256C
/WE
/CE
/OE
U7a
74ALS244AN
FFTSENDING
FFTRDYACK
U7b
74ALS244AN
PROCSENDING
PROCRDYACK
ACK2
U8
74ALS245AN
IFDATA