Dan Ports
6.111 PS2

8/10

1. a $F = B\bar{D} \oplus \overline{(A+B)C}$ ✓

$= (B\bar{D})(\overline{(A+B)C}) + \overline{(B\bar{D})}(\overline{(A+B)C})$

$= B\bar{C}\bar{D} + (\bar{B}+D)(\overline{(A+B)} + \bar{C})$

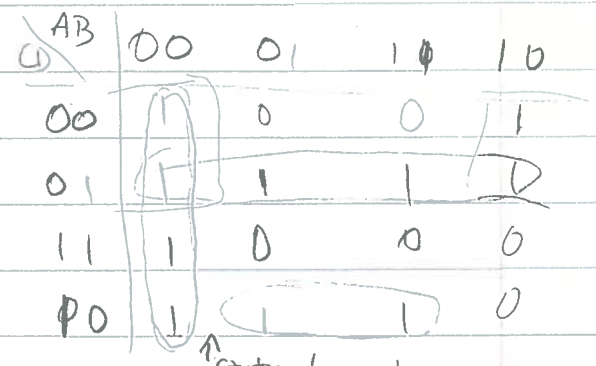
$= B\bar{C}\bar{D} + (\bar{B}+D)(\bar{A}\bar{B} + \bar{C})$

$= B\bar{C}\bar{D} + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}D$

b

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

✓



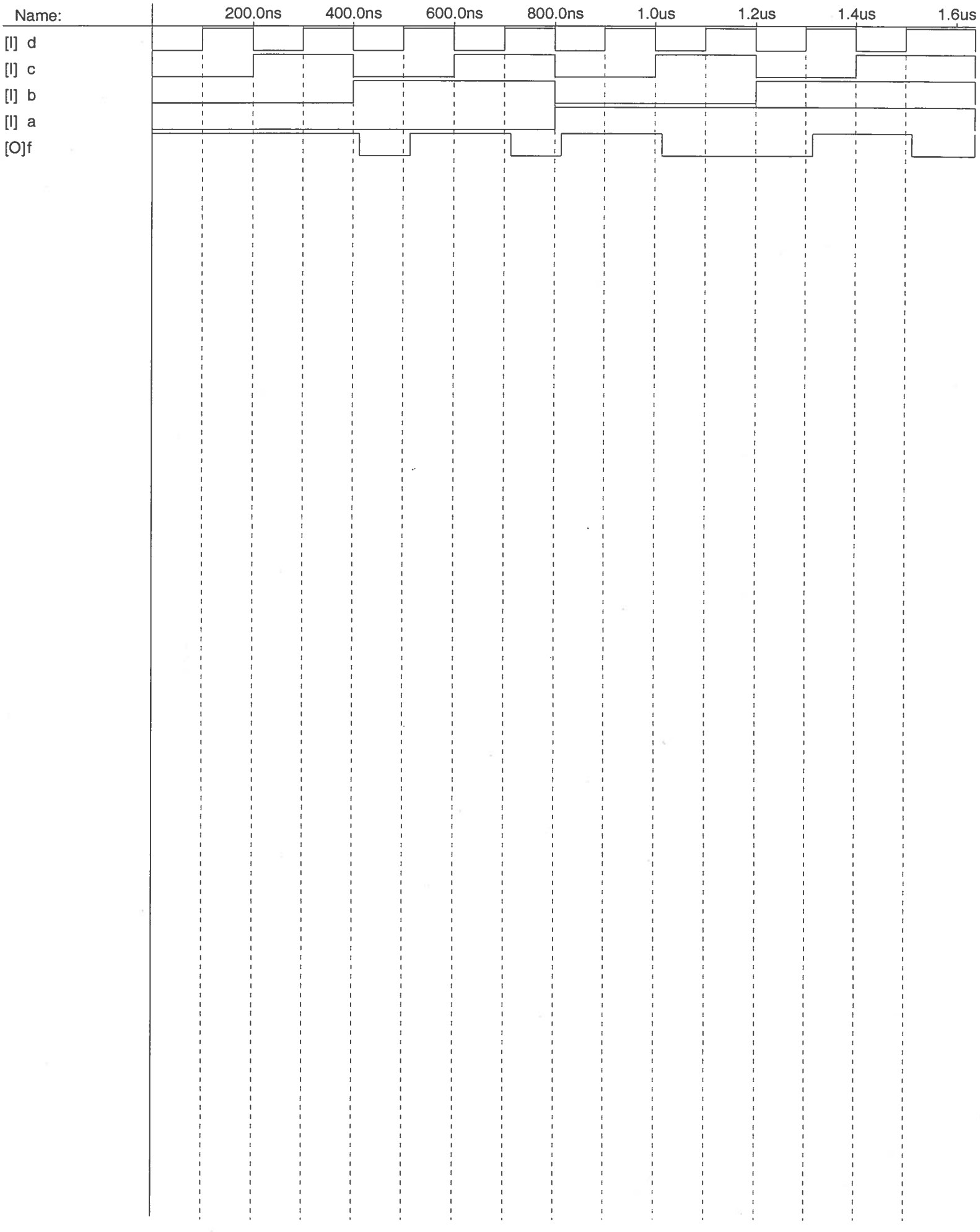
MSP: $\bar{A}\bar{B} + \bar{C}D + \bar{C}\bar{B} + B\bar{C}\bar{D}$ ✓

d. There is a static hazard when switching from $\bar{A}\bar{B}C\bar{D}$ to $\bar{A}BC\bar{D}$. This can be removed by adding a $\bar{A}C\bar{D}$ term. ✓

```
library ieee;
use ieee.std_logic_1164.all;

entity ps2 is
 port (a, b, c, d :  in std_logic;
       f : out std_logic);
end ps2;

architecture behavioral of ps2 is
begin
        f <= (b and (not d)) xor (c nand (a or b));
end behavioral;
```


Name:
200.0ns
400.0ns
600.0ns
800.0ns
1.0us
1.2us
1.4us
1.6us
[I] d
[I] c
[I] b
[I] a
[O]f

2a. The ripple counter is subject to glitches as each of the flipflops updates in sequence; e.g. the transition 011 → 100 will actually give 011 → 010 → 000 → 100. Also, the ripple counter will have a longer propagation delay due to the sequence of flipflops. Hence, the synchronous counter should be used when speed and glitch-free operation are essential. A ripple counter can be used when these are not an issue, e.g. when only using one bit of the output.

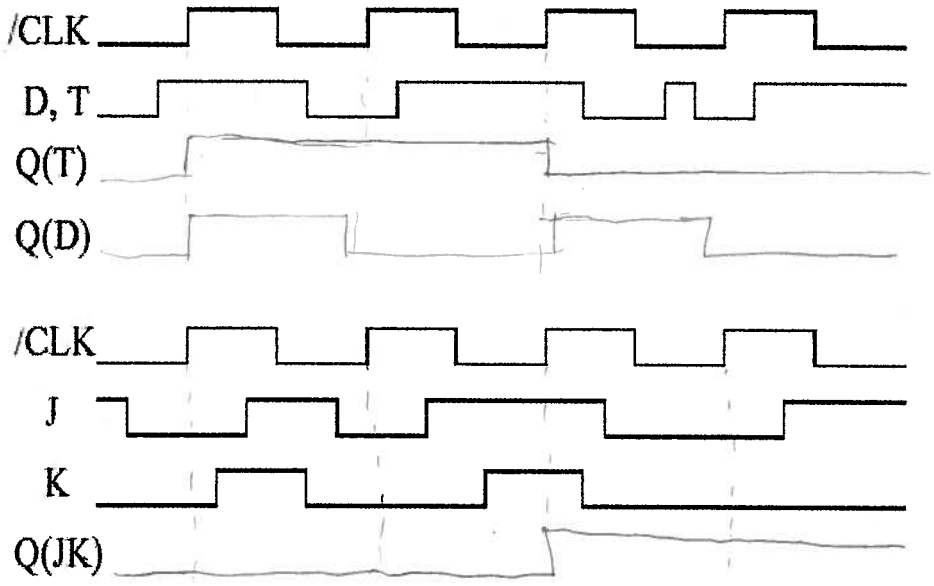
b. Both ENT and ENP must be high to enable counting. The ENP pin also disables the Ripple Carry Output.

c? -2

(c) Harvard University has hired you to design a counter to track the number of students entering and exiting a computer lab. This lab can hold a maximum of 30 students. A sensor provides two inputs: enter - pulses when 1 person enters, and exit - pulses when 1 person leaves. Your system should provide a running count of the number of students at any given time as well as a warning signal (FULL) when the maximum is reached. Assume once the max is reached no one else is allowed to enter. Design a counter circuit to implement this system and show a wiring diagram of your circuit.

Problem 3: Flip-Flops

Using the timing diagram below, draw the output of Q for a positive edge-triggered T flip-flop, positive edge-triggered D flip-flop, and a positive edge-triggered JK flip-flop. Assume that Q starts as a 0. Turn in this diagram with your solution.



should actually change on ↓

Dan Ports
6.111 PS2 - 2c
U8/Down Counter